(B) **What is claim is:**

1. A data conversion interface, comprising:

a clock signal generator generating a clock signal in response to a mode signal, said mode signal indicating operation in one of at least a first and second data length transfer mode; and

a serial-to-parallel converter receiving the clock signal, the mode signal and serial data, and converting the serial data into parallel data having a data length as set forth in the mode signal.

2. The interface of claim 1, wherein the first data length is 8 bits and the second data length is 16 bits.

3. The interface of claim 2, wherein the clock signal generator generates a mod 3 clock signal when the mode signal indicates the first data length and generates a mod 4 clock signal when the mode signal indicates the second data length.

4. The interface of claim 1, wherein the clock signal generator generates a mod 3 clock signal when the mode signal indicates the first data length and generates a mod 4 clock signal when the mode signal indicates the second data

length.

5. The interface of claim 1, wherein the serial-to parallel converter comprises:

a first transfer unit having a first storage capacity equal to said first data length, storing a first portion of the serial data and converting the stored first portion of the serial data into parallel data of the first data length;

a second transfer unit having a second storage capacity, a total of the first and second storage capacities equaling the second data length, the second transfer unit storing a second portion of the serial data and converting the stored second portion of the serial data to parallel data of a length equal to the second storage capacity.

6. The interface of claim 5, wherein the serial-to-parallel converter further comprises:

an enabling control circuit controlling whether the second portion of the serial data is one of same as and different from the first portion of the serial data based on the mode signal.

7. The interface of claim 6, wherein the enabling control circuit controls the input of serial data to the second transfer unit such that when the mode signal

indicates the first data length transfer mode, the second portion of the serial data is the same as the first portion of the serial data, and when the mode signal indicates the second data length transfer mode, the second portion of the serial data is different from the first portion of the serial data.

8. The interface of claim 5, wherein

the first transfer unit includes a first shift register having a length equal to the first data length, and shifts the serial data through the first shift register in response to the clock signal, and outputs the serial data stored in the first shift register in parallel at a predetermined interval;

the second transfer unit includes a second shift register having a length equal to the second data length minus the first data length, in a first state the second transfer unit shifts the serial data output from the first shift register through the second shift register in response to the clock signal, in a second state the second transfer unit shifts the serial data input to the first shift register through the second shift register, and the second transfer unit outputs the serial data stored in the second shift register in parallel at the predetermined interval; and

a state control unit controlling a state of the second transfer unit based on the mode signal.

9. The interface of claim 8, wherein the state control unit receives the serial data output from the first shift register, prevents the serial data output from the first shift register from being input to the second shift register when the mode signal indicates the first data length transfer mode, receives the serial data input to the first shift register, and supplies the serial data input to the first shift register to a serial input of the second shift register when the mode signal indicates the first data length transfer mode.

10. The interface of claim 9, wherein the state control unit supplies the serial data output from the first shift register to the serial input of the second shift register when the mode signal indicates the second data length transfer mode, and prevents the serial data input to the first shift register from being input by the second shift register when the mode signal indicates the second data length transfer mode.

11. The interface of claim 8, wherein the state control unit receives the serial data output from the first shift register, supplies the serial data output from the first shift register to a serial input of the second shift register when the mode signal indicates the second data length transfer mode, receives the serial data input to the first shift register, and prevents the serial data input to the first shift register from being input by the second shift register when the mode signal

indicates the second data length transfer mode.

12. The interface of claim 8, wherein the enable control circuit comprises:

a first AND gate receiving the serial data output from the first shift register and the mode signal;

an inverter inverting the mode signal;

a second AND gate receiving output from the inverter and the serial data input to the first shift register; and

an OR gate receiving output from the first and second AND gates, and an output of the OR gate connected to a serial input of the second shift register.

13. The interface of claim 8, wherein the clock generator generates the clock signal to have a first number of pulses during the predetermined interval when the mode signal indicates the first data length transfer mode, and generates the clock signal to have a second number of pulses during the predetermined interval when the mode signal indicates the second data length transfer mode.

14. The interface of claim 13, wherein the first number of pulses equals the first data length and the second number of pulses equals the second data length.

15. The interface of claim 5, wherein

the first transfer unit performs the serial-to-parallel conversion operation based on a read signal; and

the second transfer unit performs the serial-to-parallel conversion operation based on the read signal and output from the enable control unit.

16. A data conversion interface, comprising:

a clock signal generator generating a clock signal in response to a mode signal, said mode signal indicating operation in one of at least a first and second data length transfer mode; and

a parallel-to-serial converter receiving the clock signal, the mode signal and parallel data, and converting the parallel data into serial data having a data length as set forth in the mode signal.

17. The interface of claim 16, wherein the first data length is 8 bits and the second data length is 16 bits.

18. The interface of claim 17, wherein the clock signal generator generates a mod 3 clock signal when the mode signal indicates the first data length and generates a mod 4 clock signal when the mode signal indicates the

second data length.

19. The interface of claim 16, wherein the clock signal generator generates a mod 3 clock signal when the mode signal indicates the first data length and generates a mod 4 clock signal when the mode signal indicates the second data length.

20. The interface of claim 16, wherein the parallel-to-serial converter comprises:

a first transfer unit having a first storage capacity equal to said first data length, storing a least significant bits portion of the parallel data, the least significant bits portion having a width equal to the first data length, and outputting the stored least significant bits portion as serial data;

a second transfer unit having a second storage capacity, a total of the first and second storage capacities equaling the second data length, the second transfer unit storing a next most significant bits portion of the parallel data, the next most significant bits portion having a width equal to the second storage capacity, and outputting the next most significant bits portion as serial data; and

transfer control unit controlling whether the serial data output from the second transfer unit is output from the parallel-to-serial converter based on the mode signal.

22 21. The interface of claim 20, wherein

the first transfer unit includes a first shift register having a length equal to the first data length, the first transfer unit inputs the least significant bits portion into the first shift register at a predetermined interval and shifts the least significant bits portion out of the first register as serial data in response to the clock signal;

the second transfer unit includes a second shift register having a length equal to the second data length minus the first data length, the second transfer unit inputs the next significant bits portion into the second shift register at the predetermined interval, and shifts the next significant bits portion out of the second shift register as serial data in response to the clock signal; and

the transfer control unit controls whether the serial data output from the second shift register is supplied to a serial input of the first shift register.

23 22. The interface of claim 21, wherein the transfer control unit receives the serial data output from the second shift register, and prevents the serial data output from second first shift register from being input to the first shift register when the mode signal indicates the first data length transfer mode.

24 23. The interface of claim 22, wherein the transfer control unit permits

the serial data output from the second shift register to be input by the first shift register when the mode signal indicates the second data length transfer mode.

24. The interface of claim 23, wherein the transfer control unit comprises:

a first AND gate receiving the serial data output from the second shift register and the mode signal;

an inverter inverting the mode signal;

a second AND gate receiving output from the inverter and a logic level 0 voltage; and

an OR gate receiving output from the first and second AND gates, and an output of the OR gate connected to a serial input of the first shift register.

25. The interface of claim 22, wherein the transfer control unit supplies a first logic state to a serial input of the first shift register when the mode signal indicates the first data length transfer operation.

26. The interface of claim 21, wherein the clock generator generates the clock signal to have a first number of pulses during the predetermined interval when the mode signal indicates the first data length transfer mode, and generates the clock signal to have a second number of pulses during the predetermined

interval when the mode signal indicates the second data length transfer mode.

27. The interface of claim 26, wherein the first number of pulses equals the first data length and the second number of pulses equals the second data length.

28. The interface of claim 20, wherein

the first transfer unit performs the parallel-to-serial conversion operation based on a write signal; and

the second transfer unit performs the parallel-to-serial conversion operation based on the write signal and output from the transfer control unit.

29. The interface of claim 16, wherein the parallel-to-serial converter temporarily stores the parallel data, and outputs the parallel data in serial in response to a write signal, and output the parallel data in parallel in response to a read signal.

30. The interface of claim 16, further comprising:

a serial-to-parallel converter receiving the clock signal, the mode signal and serial data, and converting the serial data into parallel data having a data length as set forth in the mode signal.

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31. The interface of claim 28, wherein

the serial-to parallel converter includes,

a first transfer unit having a first storage capacity equal to said first data length, storing a first portion of the serial data and converting the stored first portion of the serial data into parallel data of the first data length,

a second transfer unit having a second storage capacity, a total of the first and second storage capacities equaling the second data length, the second transfer unit storing a second portion of the serial data and converting the stored second portion of the serial data to parallel data of a length equal to the second storage capacity, and

an enabling control circuit controlling whether the second portion of the serial data is one of same as and different from the first portion of the serial data based on the mode signal; and

the parallel-to-serial converter includes,

a third transfer unit having a third storage capacity equal to said first data length, storing a least significant bits portion of the parallel data, the least significant bits portion having a width equal to the first data length, and outputting the stored least significant bits portion as serial data,

a fourth transfer unit having a fourth storage capacity, a total of the third and fourth storage capacities equaling the second data length, the fourth

transfer unit storing a next most significant bits portion of the parallel data, the next most significant bits portion having a width equal to the fourth storage capacity, and outputting the next most significant bits portion as serial data, and

transfer control unit controlling whether the serial data output from the fourth transfer unit is output from the parallel-to-serial converter based on the mode signal.

32. The interface of claim 31, wherein

the first transfer unit includes a first shift register having a length equal to the first data length, and shifts the serial data through the first shift register in response to the clock signal, and outputs the serial data stored in the first shift register in parallel at a predetermined interval;

the second transfer unit includes a second shift register having a length equal to the second data length minus the first data length, in a first state the second transfer unit shifts the serial data output from the first shift register through the second shift register in response to the clock signal, in a second state the second transfer unit shifts the serial data input to the first shift register through the second shift register, and the second transfer unit outputs the serial data stored in the second shift register in parallel at the predetermined interval;

a state control unit controlling a state of the second transfer unit based on the mode signal;

the third transfer unit includes a third shift register having a length equal to the first data length, the third transfer unit inputs the least significant bits portion into the third shift register at a predetermined interval and shifts the least significant bits portion out of the third shift register as serial data in response to the clock signal;

the fourth transfer unit includes a fourth shift register having a length equal to the second data length minus the first data length, the fourth transfer unit inputs the next significant bits portion into the fourth shift register at the predetermined interval, and shifts the next significant bits portion out of the fourth shift register as serial data in response to the clock signal; and

the transfer control unit controls whether the serial data output from the fourth shift register is supplied to a serial input of the third shift register.